Multifunction Chip Set For T/R Module Receive Path

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Abstract

This paper presents design and test results for multifunction MMICs for C-Band Transmit/Receive (T/R) modules. This small signal chip set contains the entire receive path (5 stages of amplification and 10 passive devices) in just three chips. These IC's fabricated with the Multi-functional Self-Aligned Gate (MSAG) process, demonstrate a high level of integration, excellent performance and a good yield. The variable gain low noise amplifier has 30 ± 1 dB gain, 2.5 dB noise figure, the phase shifter/SPDT switch has 8 ± 1 dB loss and the buffer amplifier has 6.5 ± 0.2 gain and 3.5 dB noise figure. Average yield for these circuits was 40% or better.

Introduction

An active-aperture, phased-array radar consists of a large planar array of radiating elements each of which is driven by a solid-state Transmit-Receive (T/R) module. In this application thousands of T/R modules are required in each radar system with small size, low weight, low dc power consumption, high complexity and low cost [1].

The low cost of T/R modules is the driving force for the successful deployment of phased array radars[2]. GaAs MMIC technology potentially solves all of these issues except the low cost requirement as the modules are very complex. GaAs MMIC technology offers partial solutions to the cost problem as a high yield and a higher level of integration at the MMIC chip level reduces the number of chips and results in a low chip test and module assembly cost.

This paper presents the chip set for receive path of the T/R module. Figure 1 shows a block diagram of the receive path. The MMIC portion of the receive path contains all but the isolator and switch.

The signal is routed from the antenna through the isolator to a low noise amplifier(LNA). The set of attenuators following the LNA control the amplitude for both temperature compensation and beam shaping. Next an amplifier provides gain and a switch selects the receive path. The remaining circuits are used during both transmit and receive. The phase shifter sets the phase for beam shaping and finally the signal level is increased and sent to the signal processor.

Design

The circuits are placed on three MMIC chips which can be described as a variable gain LNA, a six bit phase shifter/SPDT switch and a transmit/receive buffer amplifier.

These chips are designed to be fabricated with the Multifunctional Self-Aligned Gate (MSAG) process which has a small process variation and, therefore, increases circuit yield [3]. Additionally, to increase yield, and lower cost, the chips were designed to be tolerant of process variation. Designing for process tolerance requires that the specifications are reasonable and choosing the value of the circuit elements to allow maximum variation in process sensitive elements such as FETs, resistors and tuning capacitors.

The chips were designed by using circuits similar to ones previously developed and whenever possible repeating several designs across the chip set. The

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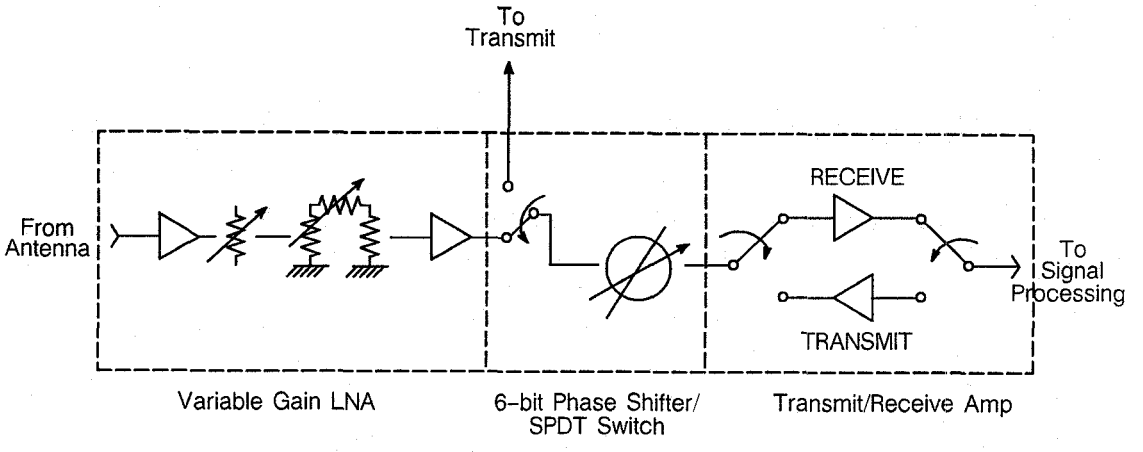

Figure 1. T/R Module Receive Path.

variable gain LNA chip is designed for 28 dB of gain in the maximum gain state and 8 dB of gain in the full attenuation state. In the maximum gain state the maximum noise figure is 2.5 dB. This chip uses a two-stage low noise amplifier, a variable attenuator, a step attenuator and a buffer amplifier as shown in Figure 1. The low noise amplifier uses series feedback in the first stage to achieve simultaneous noise match and low input VSWR. The step attenuator is a simple "T" structure tuned to maintain constant phase in the zero or eight dB states. The variable attenuator also features constant phase across a continuous attenuation range of 10 dB. This attenuator uses a dual gate FET. The buffer amplifier used as a gain block, is a simple single ended design with a little series feedback to improve noise performance.

The second chip is a six-bit phase shifter with a single pole double throw (SPDT) switch which selects the variable gain LNA chip when the module is in the receive mode. The six bits (variable bit, 11°, 22.5°, 45°, 90°, and 180°) enable the module to shift the phase from 0° to 360° within plus or minus eleven degrees. Loaded line phase shifters are used for the variable, 11, 22.5, and 45 degree bits while 90° and 180° phase shifters are of the reflection type [4]. The SPDT switch uses a simple series shunt configuration that is very broadband and process tolerant.

The transmit/receive buffer amplifier chip provides gain in either a forward or reverse direction as shown in Figure 1. This function is implemented by using two single pole double throw (SPDT) switches at each end of the chip. Therefore, either a transmit path or receive path can be selected. The transmit and receive path contain identical amplifiers with the receive amplifier having its input at the same end of the chip as the transmit output. The buffer amplifiers are identical to the one used in the variable gain LNA chip and the SPDT switches are similar to the one used in the 6- bit phase shifter chip.

Results

These three chips were fabricated using the ITT MSAG process[3]. Figures 2, 3 and 4 show a photograph of the variable gain LNA, the six bit phase shifter/SPDT switch

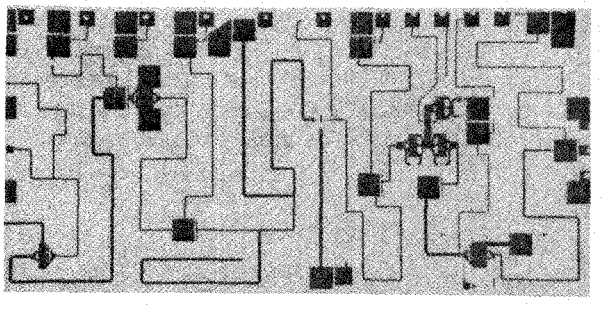

Figure 2. Photograph of Variable Gain LNA Chip.

and the transmit/receive amplifier chips. Table 1 summarizes the design requirement for the variable gain LNA and the measured results. The results listed are the average of the chip that exceeded the design requirements. The yield for this chip was 45%. The phase shifter results are listed in Table 2. All the bits worked as desired except the 180 degree bit which had a simple design error. The functional yield at this chip was about 40 percent. The transmit/receive amplifier results which are described in Table 3 are excellent with a 50 percent or greater yield. The higher yield here was probably because this chip was the least complex of the three.

Table 1- Results and Requirements For The Variable Gain LNA

Parameter	Requirements Min.	Requirements Max.	Results	Units
Frequency	5000	6000	5000-6000	MHz
Gain	28		30	dB
Gain Flatness		±1.5	±1.0	dB
Third Order Interception Point	13			dBm
VSWR (Input) VSWR (Output)		2.0:1 2.0:1	1.6:1 1.5:1	
Noise Figure		3.0	2.5	dB
Δ Gain	20		20	dB
Δ Phase		10	9	Degree

Table 2 - Results And Requirements For The 6-Bit Phase Shift/SPDT Switch

Parameters	Requirements Min.	Requirements Max.	Results	Units
Frequency	5000	6000	5000-6000	MHz
Insertion Loss 0° Phase Shift 360° Phase Shift		 11.0 11.0	 7 9	 dB dB
Amplitude Flatness Any Bit		 ±0.5	 ±0.4	 dB
Third Order Intercept Point	40			dBm
VSWR Input Output (Transmit) (Receive)		 2.0:1 2.0:1 2.0:1	 1.8:1 2.0:1 2.0:1	
Phase Accuracy		±11	±20	Degree
Switch Isolation	20		22	dB

Table 3-Results And Requirements For The Transmit/Receive Buffer Amplifier

Parameters	Requirements Min.	Requirements Max.	Results	Units
Frequency	5000	6000	5000-6000	MHz
Gain	6		6.5	dB
Gain Flatness		± 0.5	± 0.2	dB
Third Order Intercept Point	20			dBm
VSWR (Input) VSWR (Output)		2.0:1 2.0:1	1.6:1 1.6:1	
Reverse Isolation	25		30	dB
Noise Figure		4.5	3.5	dB

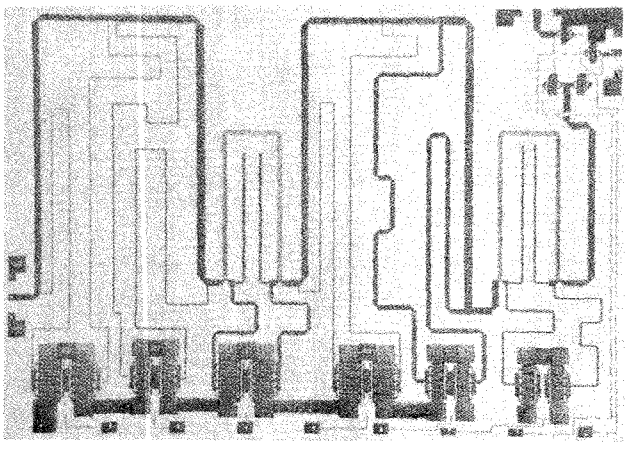

Figure 3. Photograph of 6-Bit Phase Shifter/SPDT Switch Chip.

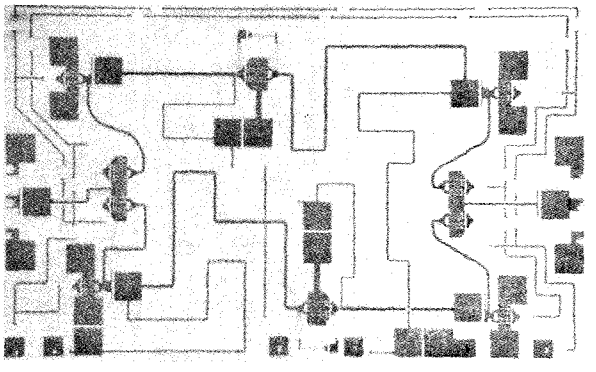

Figure 4. Photograph of Transmit/Receive Amp Chip.

Conclusion

We have successfully demonstrated a multifunction chip set for T/R modules having higher level of integration while maintaining a good yield. This chip set has reduced the receive path to three chips using a distributed matching structure. The next step is to combine all of the small signal functions onto a single chip while maintaining good yield which will lead us to manufacture low cost T/R modules.

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